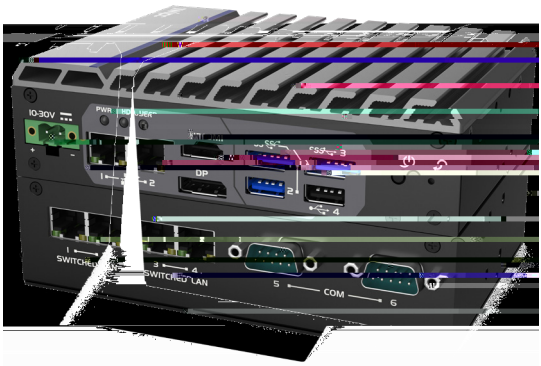
JEC-3011



Version 1.0

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2.3

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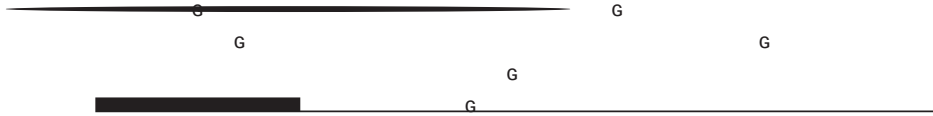
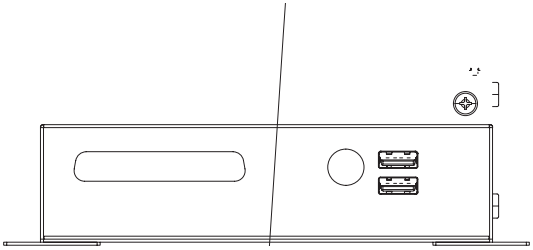




4

4.1

⚠
G

⚠
G

G I/O USB G I/O G

4.2

1. DC_IN DC
2. LAN: RJ45
3. PWR:
4. HDD:
5. USER:
6. HDMI: HDMI
7. DP: DP
8. USB3.0: USB3.0
9. USB2.0: USB2.0
10. Power Button: /
11. RESET: 4 CMOS
12. Switched LAN:
13. COM: R232/422/485
14. GPIO: GPIO
15. PS/2:
16. AUDIO:
17. ANT: WIFI

		LED	
POWER	PC		

5.5 GPIO

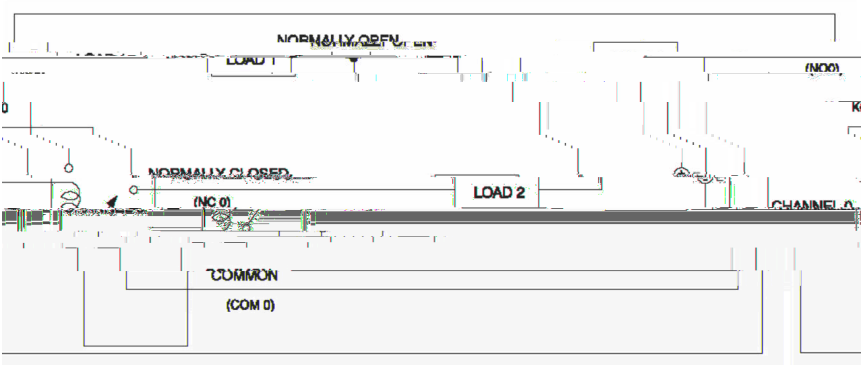
5.5.1

GPIO 8 IDI0~IDI7 10~50VDC

G

5.5.2

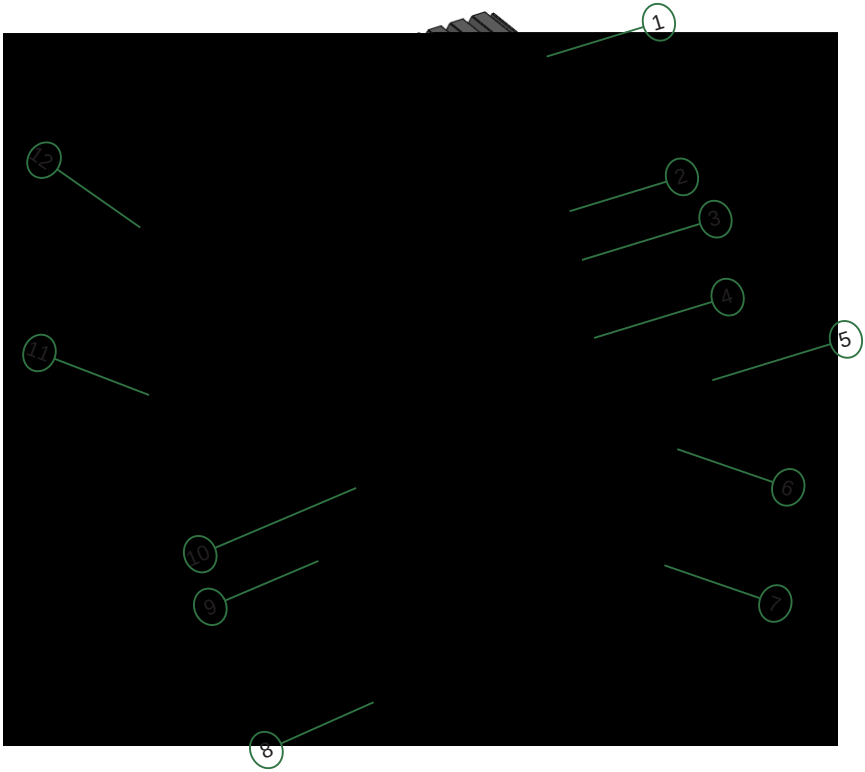
GPIO 8 G



0 d COMMON d d NORMALLY CLOSED d
1 d COMMON d d NORMALLY OPEN d G

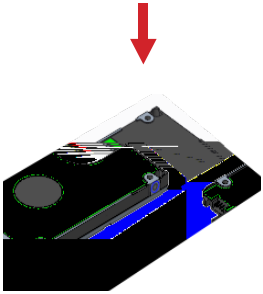
6

6.1



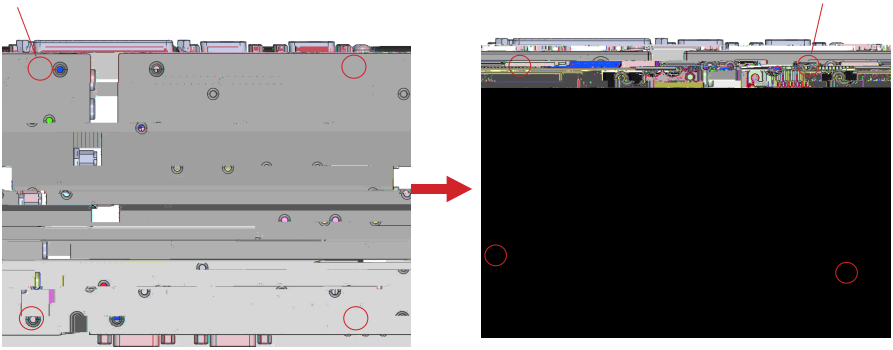
1		2		3	
4		5		6	IO
7	IO	8		9	SATA
10		11		12	

6.2



1. 4

6.3

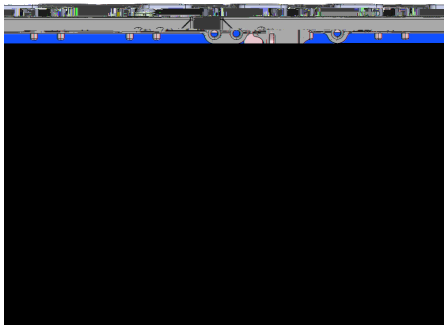


1. 4
2. 4
3. SATA G

SATA

G

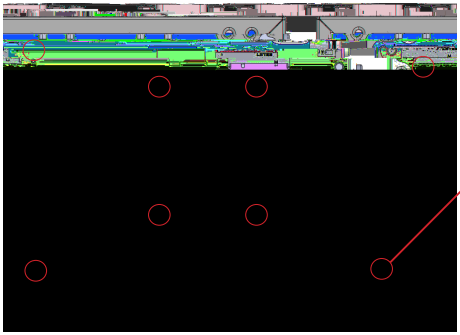
6.4 M.2 2242/2280

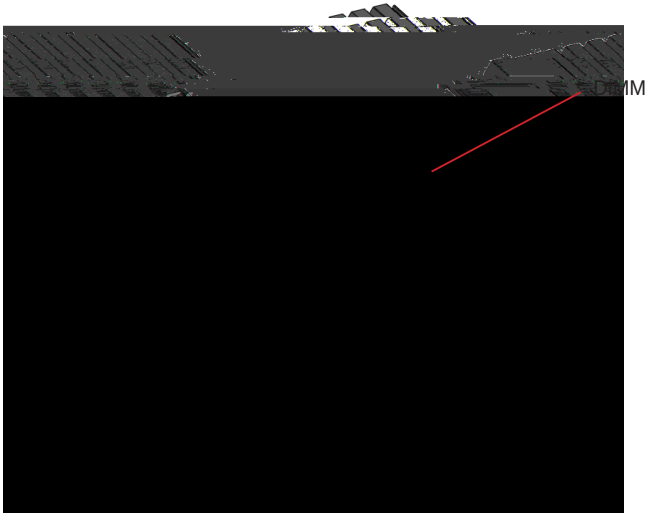


d 6.3 d G

1. 30°
2. M.2 2242 M.2 2280 M.2 2242 G

6.5



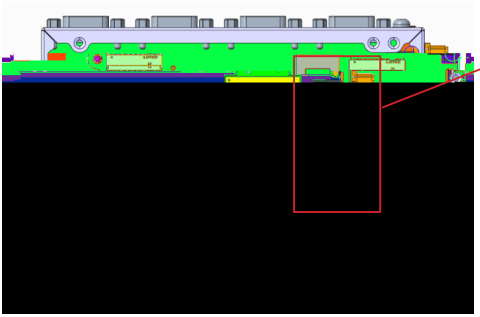


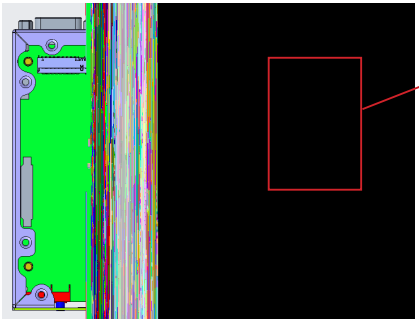
ɗ 6.3 d

1. 8 4
2. DIMM G

1. 30°
2. M.2 2242 M.2 2280 M.2 2242 G

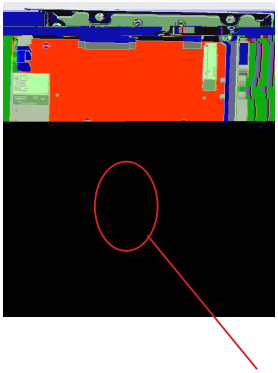
6.6 4G/5G

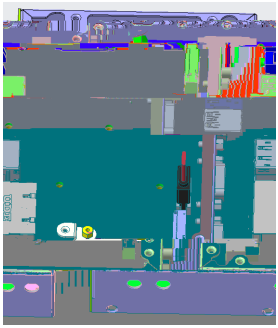




4G/5G G
4G/5G 30° G

4G 4G G





7 BIOS

7.1 BIOS

AMI BIOS BIOS Basic Input Output System (ROM Read-Only Memory) BIOS

a. POST(Power On Self Test)
b.
c. H
d. SETUP
BIOS CMOS RAM
BIOS CMOS
BIOS

7.2 BIOS

BIOS Setup BIOS

SETUP

a. SETUP
b.

BIOS BIOS

7.2.1 BIOS

<DEL> BIOS

Press <Delete> to enter SETUP

Press <F11> to enter Boot Menu

7.2.2

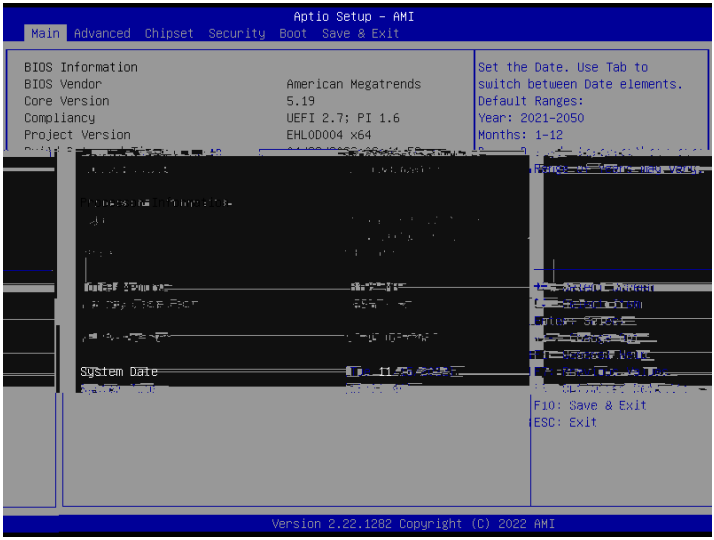
<Enter> <F1> <Esc>

← / →	
↑ / ↓	
+/ -	/
<Enter>	
<ESC>	CMOS SETUP
<F1>	
<F7>	
<F9>	
<F10>	CMOS

7.3 BIOS

Main		

7.4 Main



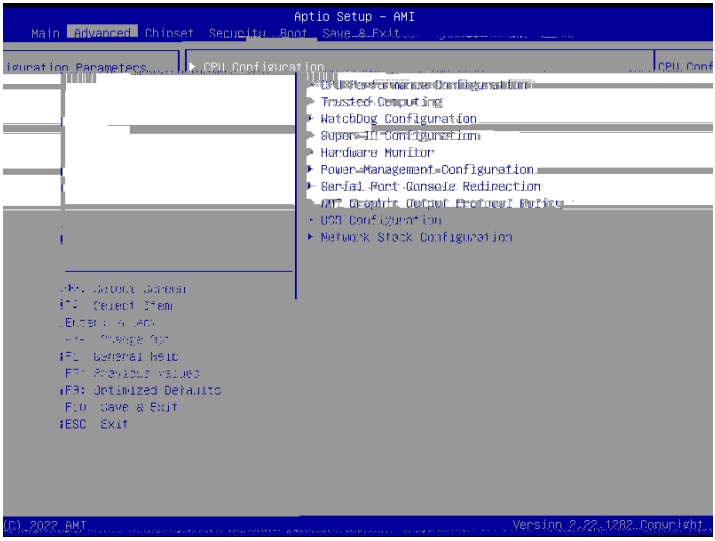
System Date ( )

, d , / / d G

System Time

< >< >< > G

7.5 Advanced



CPU Configuration	CPU	
CPU Performance Configuration	CPU	
Trusted Computing		
Watch Dog Configuration		
Super IO Configuration	Super IO	
Hardware Monitor		
Power Management Configuration		
Serial Port Console Redirection		
AMI Graphic Output Protocol Policy		
USB Configuration	USB	
Network Stack Configuration		

CPU Conf guration <Enter> G

CPU Flex Ratio Override

CPU G

Disable,Enable.

. Intel(VMX) Virtualization Technology

Intel VMX G

Disable,Enable.

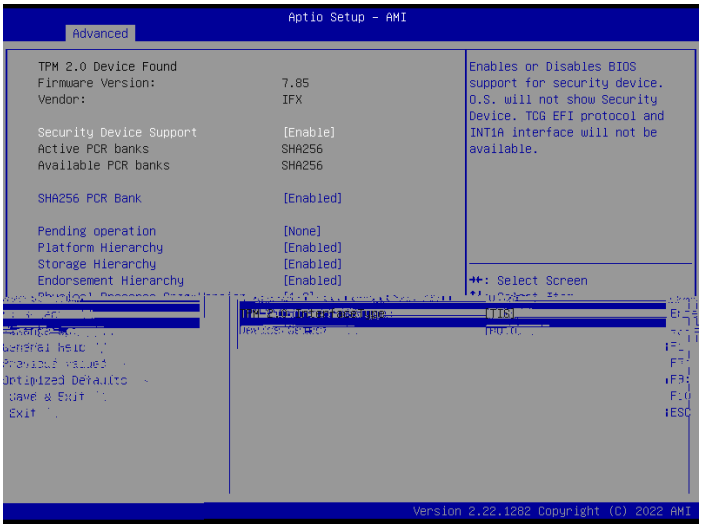
Active Processor Cores

G

ALL,1,2,3.

CPU Performance Con f guration <Enter> G

Trusted Con f guration <Enter> G



Security Device Support

BIOS G

Disable,Enable.

SHA256 PCR Bank

SHA256 PCR Bank G

Disable,Enable.

Pending Operation

srecurity G

None,TPM Clear.

Platform Hierarchy

G

Disable,Enable.

Storage Hierarchy

G

Disable,Enable.

Endorsement Hierarchy

G

Disable,Enable.

Physical Presence Spec Version

o.s. ppi G

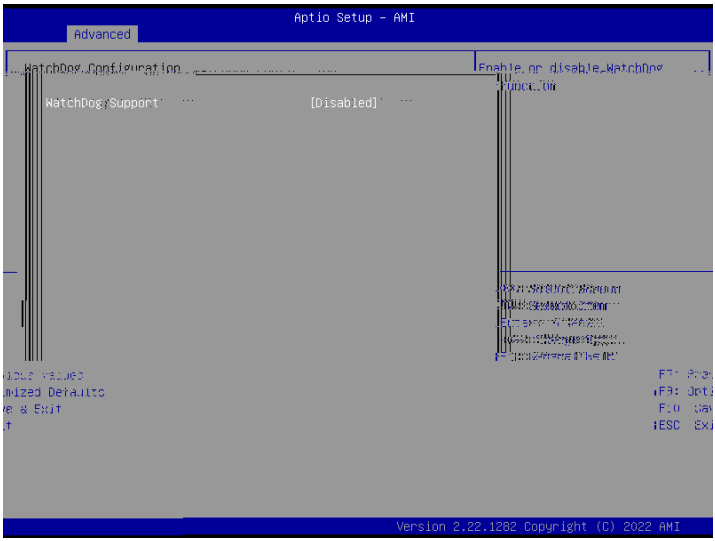
1.2,1.3.

Device Slecet

TPM G

TPM 1.2,TPM 2.0,Auto.

Watch Dog Con f guration <Enter> G

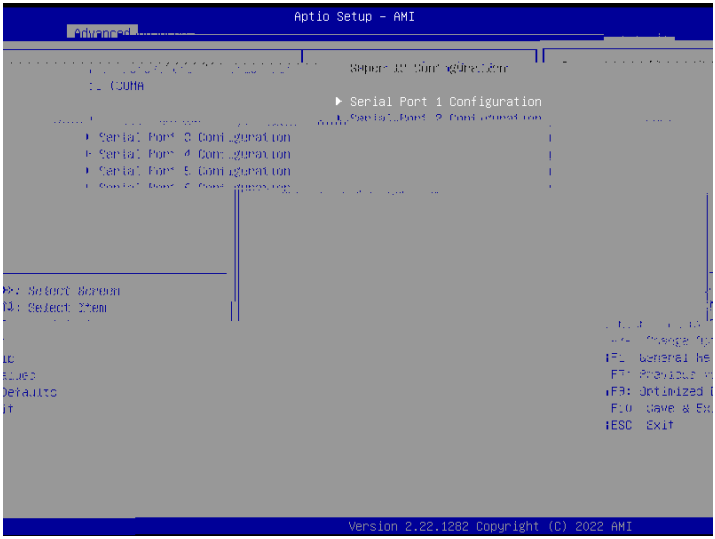


WatchDog Support

G

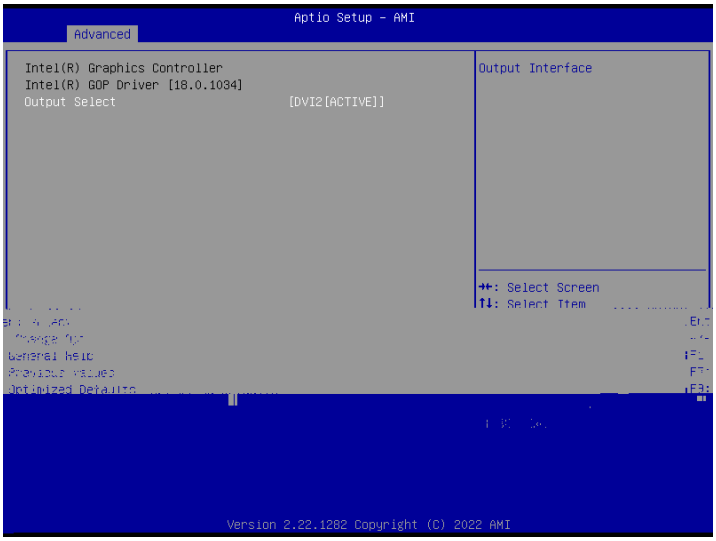
Disable,Enable.

Super IO Con f guration <Enter> G



State Ḥ

AMI Graphic Output Protocol Policy <Enter> G

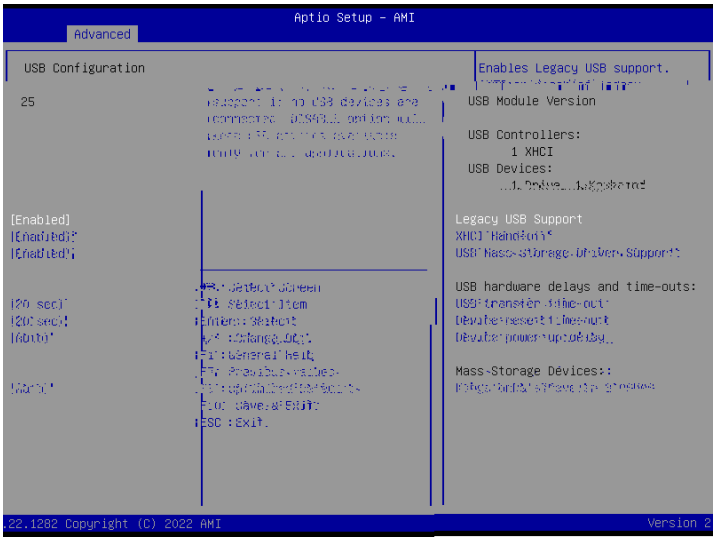


Output Select

G

DVI2[ACTIVE].

USB Confguration <Enter> G



Legacy USB Support

USB G

Disable,Enable,Auto.

XHCI Hand-of

XHCI G

Disable,Enable.

USB Mass Storage Driver Support

USB G

Disable,Enable.

USB transfer time-out

USB G

1sec,5sec,10sec,20sec.

Device reset time-out

G

10sec,20sec,30sec,40sec.

Device power-up delay

G

Auto,Manual.

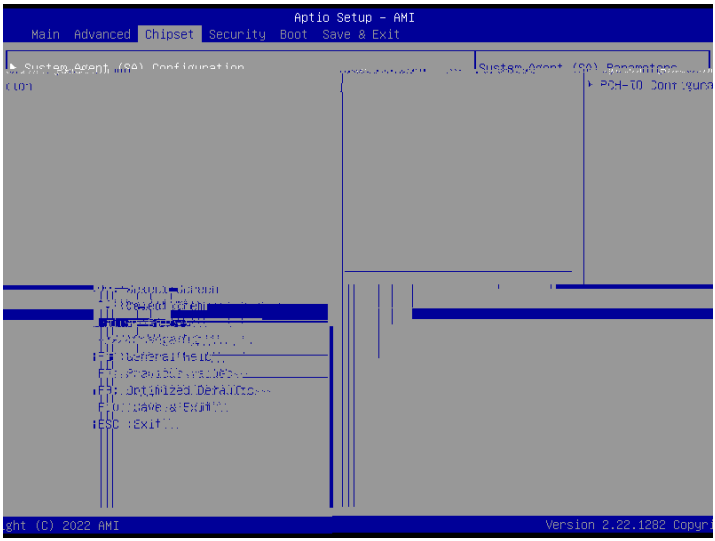
Network Stack Configuration <Enter> G

Network Stack

CSM G

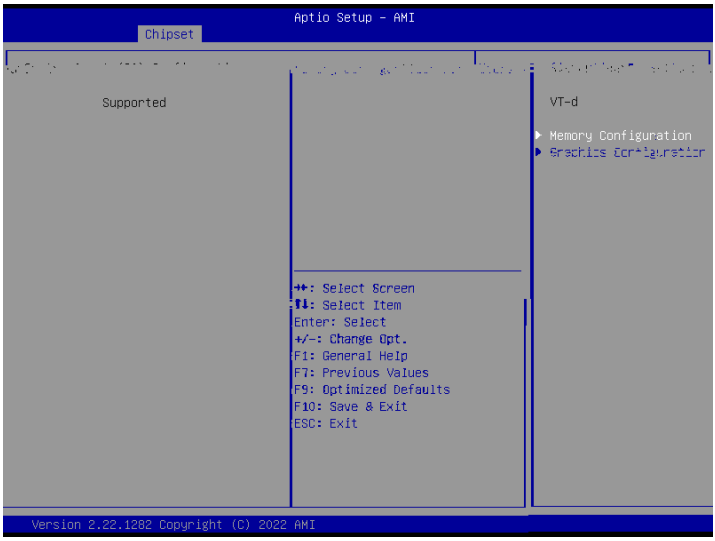
Disable,Enable.

7.6 Chipset



System Agent SA) Con guration	SA	
PCH-IO Con guration	PCH-IO	

System Agent(SA) Conf guration <Enter> G



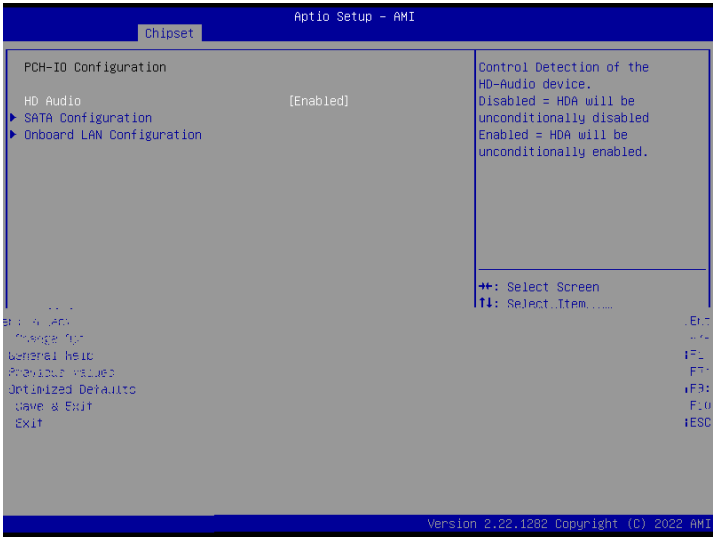
Memory Conf guration

G

Graphics Conf guration

G

PCH-IO Conf guration <Enter> G



HD Audio Con f guration

G

Disable,Enable,Auto.

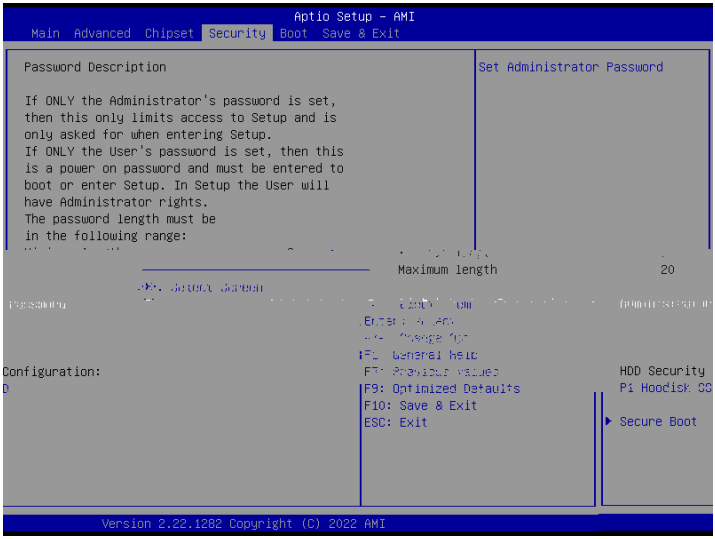
SATA Con f guration

SATA G

Onboard LAN Con f guration

G

7.7 Security



Administrator Password

1. Administrator Password <Enter> G
2. d Create New Password d 3~20 <Enter> d Con f rm Password d G d Invalid Password! d G d Administrator Password d d Enter Current Password d d Create New Password d <Enter> G

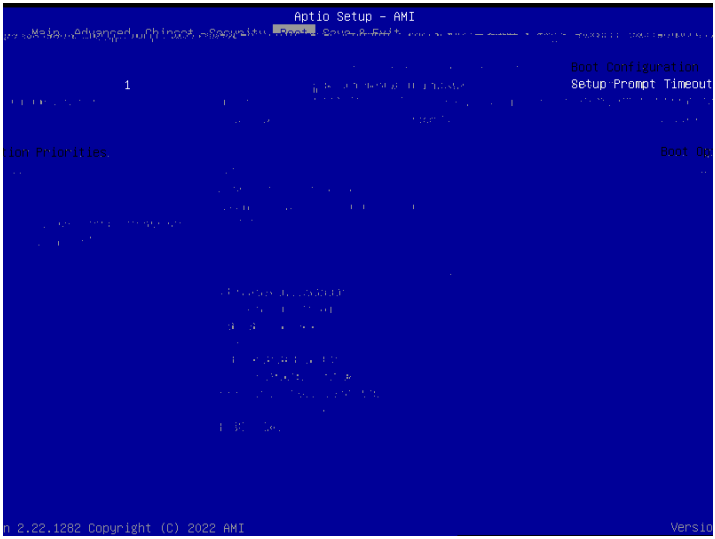
P1:Hoodisk SSD

HDD G

Secure Boot

G

7.8 Boot



Setup Prompt Timeout

G

Boot NumLock State

NumLock G

On,Of.

Quiet Boot

G

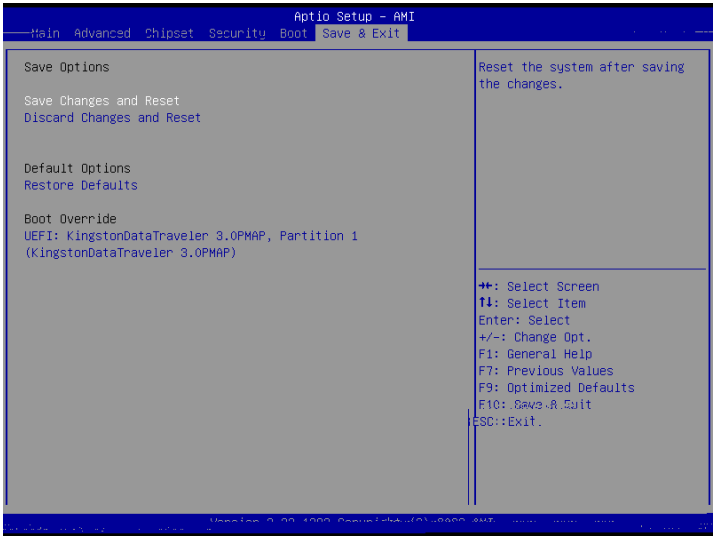
Disable,Enable.

Boot Option #1

1 G

Kingston Data Traveler 2.01.00,Disable.

7.9 Save&Exit



Save Changes and Reset

G

Discard Changes and Reset

G

Restore Defaults

G

8.2 GPIO

AIoT-EHL GPIO
1 GP30/31/32/37/63/64/65/86 G

2 GP33/34/35/36/40/41/42/43/82 G

3 GPIO Group GP3x/4x/6x Logical Device 7 GP8x Logical Device 9
4 GP3x(30~37) Logical Device 7 Register
0xED Bit0 Bit7 GP4x(40~47) Logical Device
7 Register 0xF1 Bit0 Bit7 GP6x(60~67) Logical Device 7 Register
0xF9 Bit0 Bit7 GP8x(80~87) Logical Device 9 Register 0xF1 Bit0
Bit7;
5 GPIO Group3 H GPIO Group4/6
GPIO_GROUP_3_DATA_REGISTER GPIO Group4/6 H0x30/0x37 0x40/0x47
0x60/0x67 GPIO Group 8 Group4/6
d //b. d GPIO_LDN7_DEVICE GPIO_LDN9_DEVICE G

```
#define SuperIo_Index_Port 0x2E
#define SuperIo_Data_Port 0x2F
#define GPIO_LDN7_DEVICE 0x07
#define GPIO_LDN9_DEVICE 0x09
#define GPIO_GROUP_3_DATA_REGISTER 0xED
#define GPIO_GROUP_4_DATA_REGISTER 0xF1
#define GPIO_GROUP_6_DATA_REGISTER 0xF9
#define GPIO_GROUP_8_DATA_REGISTER 0xF1
```

GPIO Group 3

```
//a. Super IO Configuration Mode
IoWrite8(SuperIo_Index_Port, 0x87);
IoWrite8(SuperIo_Index_Port, 0x87);

//b. GPIO, LDN 7
IoWrite8(SuperIo_Index_Port,0x07);
IoWrite8(SuperIo_Data_Port,GPIO_LDN7_DEVICE);

//c. GPIO Group 3
UINT8 BitOffset;
UINT8 GpioNumber;
UINT8 Data8
for(GpioNumber=0x30; GpioNumber<=0x37; GpioNumber++)
{

BitOffset = GpioNumber - 0x30;
IoWrite8(SuperIo_Index_Port, GPIO_GROUP_3_DATA_REGISTER);
Data8 = IoRead8(SuperIo_Data_Port);
Data8 = Data8>>BitOffset;
Data8 = Data8 &0x1;
}
if(Data8&0x1){
```

```
return 1;//        GPIO
}else{
return 0;//        GPIO
}

//d.    GPIO Group 3                    GPO              GPIO              GPI

for(GpioNumber=0x30; GpioNumber<=0x37; GpioNumber++)
{
BitOfset = GpioNumber - 0x30;
IoWrite8(SuperIo_Index_Port, GPIO_GROUP_3_DATA_REGISTER);
Data8 = IoRead8(SuperIo_Data_Port);
Data8 &=~(0x1<<BitOfset);//       bit       0          GPIO
//Data8 |= (0x1<<BitOfset); /*       bit          1          GPIO                */
IoWrite8(SuperIo_Data_Port,Data8);//
}

//f.       Super IO    Configuration Mode
IoWrite8(SuperIo_Index_Port, 0xAA); //       Super IO Configuration Mode       SuperIO
                                ,                  Configuration Mode G
```

8.3 WDT

```
#define SuperIo_Index_Port                0x2E
#define SuperIo_Data_Port                 0x2F
#define GPIO_LDN8_DEVICE                  0x08
UINT8 Data8

//a.       Super IO    Configuration Mode
IoWrite8(SuperIo_Index_Port, 0x87);
IoWrite8(SuperIo_Index_Port, 0x87);

//b.                  GPIO, LDN 8
IoWrite8(SuperIo_Index_Port,0x07);
IoWrite8(SuperIo_Data_Port,GPIO_LDN8_DEVICE);

//c. Enabled WDT
IoWrite8(SuperIo_Index_Port,0x30);
IoWrite8(SuperIo_Data_Port,IoRead8(SuperIo_Data_Port)|0x01);

//d.       WDT                    Register 0xF0    Bit3          1                    0
IoWrite8(SuperIo_Index_Port,0xF0);
//
IoWrite8(SuperIo_Data_Port,IoRead8(SuperIo_Data_Port)|0x08);
//
// IoWrite8(SuperIo_Data_Port,IoRead8(SuperIo_Data_Port)&0xF7);
```

```
//e.      WDT
/*xx                                  0   255 G      0      WDT                          WDT
                          G      WDT                                                  5
                                                                                  */
Data8 = xx;
IoWrite8(SuperIo_Index_Port,0xF1);
IoWrite8(SuperIo_Data_Port,Data8);

//f.
                    d //e. d              0xF1              G
Data8 = xx;
IoWrite8(SuperIo_Index_Port,0xF1);
IoWrite8(SuperIo_Data_Port,Data8);

//g.      WDT
/*                              WDT                              WDT
                */
Data8 = 0x00;
IoWrite8(SuperIo_Index_Port,0xF1);
IoWrite8(SuperIo_Data_Port,Data8);

//h.      Super IO   Configuration Mode
IoWrite8(SuperIo_Index_Port, 0xAA); //      Super IO Configuration Mode      SuperIO
                          ,                Configuration Mode G
```

9

G

G

10

10.1

		/
		1Hʊ 2Hʊ 12
	ɗ ɗ	
		ɢ
		1Hʊ 2Hʊ